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Telairity Semiconductor Launches Telairity-1: Real-Time H.264 High-Definition Video Architecture Delivers Highest Level of Video Processing Available in a Single Chip

STANFORD, Calif.—August 15, 2005—A breakthrough processor architecture for high-definition (HD) video encoding was announced today at Hot Chips 17 by Santa Clara-based Telairity Semiconductor.

Harnessing multiple independent vector/scalar cores, the multicore Telairity-1 architecture is specifically designed to handle the demanding computational requirements of the H.264 (MPEG-4 Part 10) HD codec. H.264 is set to supersede MPEG-2 as the standard by which HD video is compressed in the professional broadcast environment for transmission, storage, and editing, where the new standard will deliver the same or better picture quality with a lower bit rate.

Beginning with the T1P2000 multicore video processor, the first system-on-chip (SoC) to be built using the new architecture, H.264 encoding solutions implemented with Telairity-1 will offer the smallest footprint and lowest cost for broadcast-quality H.264 video compression, requiring typically less than one quarter the number of chips of general-purpose DSPs solutions.

"The best processor benchmark is the customer's application, and it is in this type of environment that we've designed and measured the capabilities of Telairity-1 to deliver the highest level of video processing available in a single chip," said Howard Sachs, founder, president and CEO of Telairity Semiconductor. "Lower prices for HD equipment, ramping sales of HDTV receivers and monitors, and the availability of HD-DVD and Blu-Ray DVD players mean that HDTV has arrived. Now the industry is positioned to ensure that the reality of HDTV will live up to the audience's expectations. Encoders designed with Telairity-1 processors will play a major role in making this happen."

A very powerful processor is required to implement the H.264 algorithm. An H.264 compression engine requires 4 to 6 times the computational power of an MPEG-2 compression engine.

The programmable Telairity-1 architecture delivers this power by combining five independent vector/scalar cores, a video controller, and a DRAM

controller supporting an I/O bandwidth up to 5.3 Gbps in a single multicore SoC. Each vector/scalar core features four vector pipes with independent hardware, an independent scalar unit, 128 Kbytes of on-chip vector SRAM, a 4 Kbyte vector SRAM data cache, an 8 Kbyte scalar scratchpad memory, and a 32-Kbyte instruction cache. As a fully programmable chip, Telairity-1 will allow customers to modify or add new algorithms to customize or improve the encoder over time.

At a clock rate of 668.25 MHz, or nine times the 74.25-MHz 20-bit video standard, the T1P2000, first product implemented on the new architecture, achieves a total sustained chip performance of 55.5 GOP (Giga operations) per second.

"H.264 is an important new standard for HD broadcasting, and Telairity has positioned itself well with this architecture to take advantage of the demand for H.264 encoding equipment," said Michelle Abraham, Principal Analyst, Converging Markets & Technologies, Multimedia, at In-Stat.

Used at the heart of professional broadcast encoding solutions, the Telairity-1 T1P2000 will allow designers to build high-quality encoders with fewer chips at the board level, which translates into better reliability and lower production costs for OEMs. Where a general-purpose, 600-MHz to 1-GHz DSP based real-time H.264 encoder implementation would require 18 to 32 DSPs and 6 or more FPGAs, the Telairity solution requires only four to eight Telairity video processor chips and one small FPGA to achieve equivalent bit rates.

Flexibility is another bottom-line benefit Telairity-1 delivers. Devices built on this architecture can be used for many different video encoding applications, allowing OEMs to use the same platform to deliver a range of functional capabilities. Beyond professional broadcast applications, the Telairity-1 processor will be used to enable HD video applications in video conferencing, security and surveillance, and medical imaging systems.

Packaged in the 1156-pin FCBGA (flip chip ball grid array) package, samples of the first Telairity-1 product, the 668.25-MHz T1P2000, are available now, with production quantities available in Q4 2005. Pricing in 10,000-piece quantities for U.S. delivery will start at $425.

Editor resources:

Links to product datasheet:
http://www.telairity.com/downloads/v1.01 T1 Video processor.pdf

Link to product photo:
http://www.wallstreetcom.tv/telairity/t1p2000.zip

About Telairity Semiconductor
Telairity Semiconductor delivers solutions for high-definition (HD) broadcast-quality video applications. Products built on the company's Telairity-1 real-time HD video architecture deliver the industry's highest level of video processing available on a single chip and address emerging standards for video compression including H.264. Telairity supplies highly integrated, complete hardware and software solutions that enable OEMs to get to market quickly with cost effective, high reliability and high-quality encoding systems. Telairity products address a number of markets, including broadcast encoders, video servers, video edit and authoring systems, video conferencing, and security and surveillance. The company was founded in 2001 and is based in Santa Clara, California.