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Better Technology Top to Bottom: The Telairity Edge

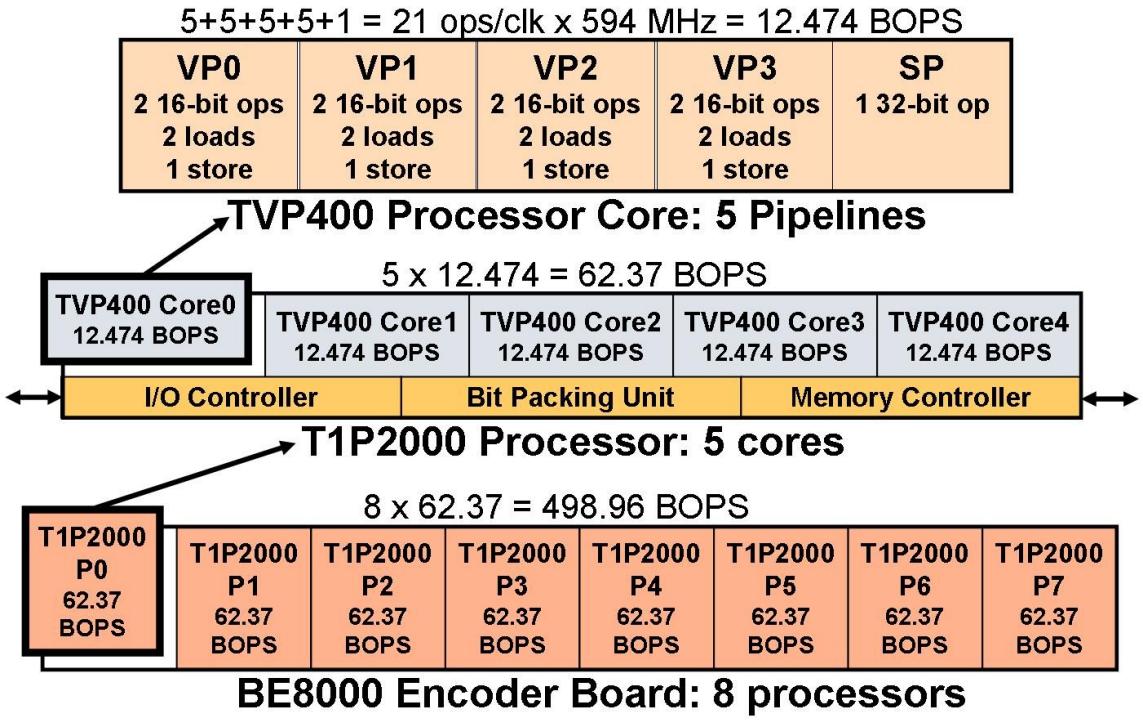
For the most part, companies that develop professional broadcast encoders fall into one of three groups, when considered in light of the technologies employed to develop systems.

- Some companies adopt a commercial encoder chip (like the Ambarella A2), developed for a related but distinct and much higher volume market (e.g., cameras), and build encoders around that base "System on a Chip" (SoC) hardware platform.
- Other companies adopt a general purpose CPU (like the latest Intel or AMD quad-core generation of x86 processor), and implement encoders in software on a PC hardware platform—perhaps using some add-in video accelerator board.
- A third group of companies eschews both of these approaches (special-purpose SoCs or general-purpose CPUs), and develops encoders around some combination of commercially available DSPs (from vendors like TI) and FPGAs (from vendors like Xilinx).

Prominent among Telairity's several distinctions is the fact that it uses none of the technical strategies listed above for product development. Instead, Telairity has leveraged its roots in the semiconductor industry, together with its patented technology for developing complex ASICs with small hardware design teams in a relatively short time, to create the 594 MHz Telairity T1P2000 video processor, targeted to video encoding. To complement this unique hardware platform, Telairity also has invested in an elite software development team, tasked with creating AVClairity encoding software, expressly designed to run directly on the T1P2000 video processor—avoiding the overhead of an operating system on the one hand, while harnessing all the horsepower available on the T1P2000 chip on the other hand. A third, tightly-knit design team creates the systems that ultimately incorporate both Telairity video processors and AVClairity encoding software, all the way from board design through sheet metal enclosures.

The result of this top-to-bottom investment in technology is uniquely powerful, uniquely fast, and unusually reliable encoding platforms. Each T1P2000 video processor chip implements five identical, loosely-coupled TVP400 processing cores. Each TVP400 core, in turn, comprises five separate execution engines: 4 vector pipelines and a scalar pipeline. Although the lone scalar engine is a simple 32-bit RISC design, capable of dispatching one instruction every clock cycle, the four 16-bit vector engines are each capable of executing up to five operations per clock cycle: 2 arithmetic-logical operations, 2 loads, and 1 store. Summing up the potential operations performed per core, per chip, and per board in a Telairity HD encoder design yields a staggering total of nearly 500 billion operations per second, as shown in Figure 1.

The 16-bit length of vector operations reflects the fact that over 90% of all multimedia data is 16-bits or less in length. Exceptions to this rule can be handled either by the 32-bit scalar engine in each core, or by chaining two of the 16-bit vector units together. And, since a single vector instruction can trigger anywhere from 1 to 32 sequential operations, the highly parallel, multicore, multipipe architecture of the T1P2000 chip is a perfect match for many of the repetitious (indeed, tedious) operations involved in video compression.



This includes the most compute-intensive motion estimation and motion compensation tasks performed on the multiple, adaptive macroblock sizes allowed by AVC coding. The 4x4 block intra-prediction algorithm, for example, calculates eight modes simultaneously, using the two arithmetical operations supported by each of the 4 vector pipes in a core—fully 8X faster than this particular algorithm could run on a single scalar unit.

In short, a Telairity-designed board based on Telairity's purpose-built T1P2000 video processor yields enormous raw horsepower, efficiently applied to H.264/AVC compression by Telairity's custom AVClairity encoding software. The result is extraordinarily powerful encoding systems, capable of generating quality images using minimal bits in just a few frames of latency. The efficiency of Telairity systems is marked by the fact that they dissipate relatively little heat (contributing to their reliability, since heat is a leading cause of electronic component failure), run quietly, and boot up within three seconds of power on. Indeed, enough room is left over inside the compact 1RU system enclosure used for all Telairity encoders to allow for optional dual redundant power supplies, further augmenting the overall robustness of Telairity systems.

The fact that encoder functions are implemented in Telairity's AVClairity software, rather than hardwired into the T1P2000 video processor, makes Telairity encoders fully field upgradeable via a simple download. At the same time, the fact that the Telairity's AVClairity encoder software runs directly on Telairity's T1P2000 video processor, without any need for an intervening operating system, reduces the latency of all encoding operations, improves system responsiveness, and at the same time eliminates a significant potential source of problems.

Taken together, the direct consequence of Telairity's top-to-bottom investment in encoding technology is a family of HD and SD H.264/AVC encoders that offer customers a value proposition unmatched by any other H.264/AVC encoders available on the market today.